CircuitClarity RESOURCE

Serial-bus timing and termination

https://circuitclarity.com/resources/serial-bus-timing-and-termination/

The decision this guide supports

A serial bus works only when every connected device shares the electrical margin. Pullups, capacitance, timing, thresholds, termination, and topology must be evaluated as a system instead of borrowed from one data sheet.

A useful calculation is not the finish line. It becomes useful when its method, units, source conditions, and omitted effects fit the actual design question. Use this reference to identify that boundary before treating a nominal result as an implementation decision.

DECISION MAP

From first estimate to defensible next step

1. **Collect limits for every transmitter, receiver, and bus mode.**
   Start by naming the physical quantity, operating condition, and decision at stake. A number without that context cannot establish a design margin.

2. **Estimate loading from traces, cables, inputs, and fixtures.**
   Keep this check explicit. It separates a useful first-pass model from an answer that only looks precise.

3. **Calculate timing or pullup constraints as an interval.**
   Keep this check explicit. It separates a useful first-pass model from an answer that only looks precise.

4. **Measure edge timing and logic levels on the assembled bus.**
   Treat this as the handoff point. Compare the result with selected-part evidence, the real layout or assembly, and a measurement method that can reveal the remaining uncertainty.

Worked design review

Consider a designer using this method to make a first selection. The initial estimate establishes the nominal target, but it should not silently absorb a rating, curve, parasitic, temperature condition, or measurement setup from a different scenario. The correct outcome is often not a single chosen value: it is a short list of conditions that must be satisfied together.

Begin with the first two steps above, then ask whether the value still fits when the most consequential real-world condition changes. If it does, the estimate has earned a more detailed check. If it does not, the discrepancy identifies the design variable that deserves attention before a board, part, or test plan is committed.

> **Practical interpretation**
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> A resistor calculation does not prove protocol compliance or signal quality in a physical assembly. That is not a weakness in the method. It is the cue to use the correct next source of evidence.

Questions to take into a design review

- Does the pullup or termination calculation account for the total capacitance of every device and cable segment on the shared bus, not just one device?
- Has the timing margin been checked at the product's full rated temperature range, not only at room temperature?
- Has the calculated result been confirmed with a measurement of edge timing and logic levels on the actual assembled bus?

These questions prevent a common failure mode: moving a correct equation into a context where its assumptions no longer hold. They also make it easier for another engineer to reproduce the reasoning and identify which condition needs more evidence.

Common ways this reasoning goes wrong

Sizing a pullup resistor from one device's data sheet without summing total bus capacitance

The correct pullup range depends on the capacitance of every device, connector, and trace length on the shared bus, not just the capacitance of the device being added most recently.

Assuming a bus timing margin calculated at room temperature holds at temperature extremes

Logic threshold and propagation-delay specs typically carry their own temperature range; a margin that looks comfortable at 25°C can shrink meaningfully at a product's rated temperature extremes.

Treating a passing calculation as equivalent to a passing physical measurement

A calculation only reflects the parasitics that were entered into it. The final check on a serial bus is measured rise time and logic levels on the actual assembled hardware, not just the arithmetic.

Where this guide stops

A resistor calculation does not prove protocol compliance or signal quality in a physical assembly.

For a consequential design, preserve the inputs and conditions used here, then compare them with the selected component or system evidence. That makes the follow-up review faster and keeps a useful first estimate from becoming an unsupported claim.

Frequently asked questions

▶ **Why does my I2C bus work with two devices but fail once I add a third?**

▶ **Do all devices on a shared bus need to support the same bus speed mode?**

▶ **Why measure the bus after calculating pullup and timing values on paper?**

Related engines

- **I2C pullup resistor designer**
- **SPI timing-margin analyzer**
- **CAN bus termination planner**
- **RS-485 bias and termination designer**

Method authorities and source conditions

Use this guide alongside the engine-specific method and selected component or system data. The underlying reference families are NXP I2C references, TI I2C references. Those sources establish condition-specific behavior; CircuitClarity uses them to frame the decision and its limits.