CircuitClarity RESOURCE

Oscillator and clock accuracy budgets

https://circuitclarity.com/resources/oscillator-and-clock-accuracy/

The decision this guide supports

Initial tolerance, load pulling, temperature, aging, jitter, divider quantization, and system timing requirements are separate clock-error mechanisms.

A useful calculation is not the finish line. It becomes useful when its method, units, source conditions, and omitted effects fit the actual design question. Use this reference to identify that boundary before treating a nominal result as an implementation decision.

DECISION MAP

From first estimate to defensible next step

1. **List every entered error mechanism: initial tolerance, temperature, aging, and load pulling.**
   Start by naming the physical quantity, operating condition, and decision at stake. A number without that context cannot establish a design margin.

2. **Combine bounded, signed contributors by worst-case addition for a total ppm range.**
   Keep this check explicit. It separates a useful first-pass model from an answer that only looks precise.

3. **Add jitter as a separate, RSS-combined term when it affects the specific decision.**
   Keep this check explicit. It separates a useful first-pass model from an answer that only looks precise.

4. **Compare the total error against the actual system timing requirement.**
   Treat this as the handoff point. Compare the result with selected-part evidence, the real layout or assembly, and a measurement method that can reveal the remaining uncertainty.

Worked design review

Consider a designer using this method to make a first selection. The initial estimate establishes the nominal target, but it should not silently absorb a rating, curve, parasitic, temperature condition, or measurement setup from a different scenario. The correct outcome is often not a single chosen value: it is a short list of conditions that must be satisfied together.

Begin with the first two steps above, then ask whether the value still fits when the most consequential real-world condition changes. If it does, the estimate has earned a more detailed check. If it does not, the discrepancy identifies the design variable that deserves attention before a board, part, or test plan is committed.

> **Practical interpretation**
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> Frequency-accuracy ppm error and short-term jitter are different mechanisms; combining them incorrectly overstates or understates the real timing risk. That is not a weakness in the method. It is the cue to use the correct next source of evidence.

Questions to take into a design review

- Have jitter and long-term ppm frequency accuracy been tracked as separate terms, not combined into one number?
- Was the actual board load capacitance checked against the crystal's specified load capacitance, not assumed to match by default?
- Were bounded, signed error contributors combined by worst-case addition rather than RSS?

These questions prevent a common failure mode: moving a correct equation into a context where its assumptions no longer hold. They also make it easier for another engineer to reproduce the reasoning and identify which condition needs more evidence.

Common ways this reasoning goes wrong

Treating jitter and long-term frequency-accuracy ppm as the same error mechanism

These describe different timing behaviors (long-term average offset versus short-term variation) and are used to answer different design questions; substituting one for the other in a budget produces a misleading result.

Ignoring load-capacitance mismatch as a source of frequency error

A crystal only hits its rated frequency at its specified load capacitance; a board's actual load capacitor values and stray capacitance need to be checked against that specification, not assumed correct by default.

Combining bounded, signed error terms with RSS instead of worst-case addition

Manufacturer-specified bounded terms like initial tolerance and temperature drift are not independent random variables; RSS-combining them can understate the real worst-case total error.

Where this guide stops

Frequency-accuracy ppm error and short-term jitter are different mechanisms; combining them incorrectly overstates or understates the real timing risk.

For a consequential design, preserve the inputs and conditions used here, then compare them with the selected component or system evidence. That makes the follow-up review faster and keeps a useful first estimate from becoming an unsupported claim.

Frequently asked questions

▶ **Is jitter just another way of expressing frequency-accuracy error in ppm?**

▶ **Does crystal load capacitance really affect frequency accuracy?**

▶ **Why combine some clock-error terms by worst case and not all of them by RSS?**

Related engines

- **UART baud-rate error**
- **PWM frequency and resolution planner**
- **PLL frequency planner**
- **DDS tuning-word calculator**
- **Crystal load-capacitor selector**
- **Oscillator ppm and frequency-error budget**

Method authorities and source conditions

Use this guide alongside the engine-specific method and selected component or system data. The underlying reference families are Analog Devices RF references, Analog Devices toolbox references. Those sources establish condition-specific behavior; CircuitClarity uses them to frame the decision and its limits.